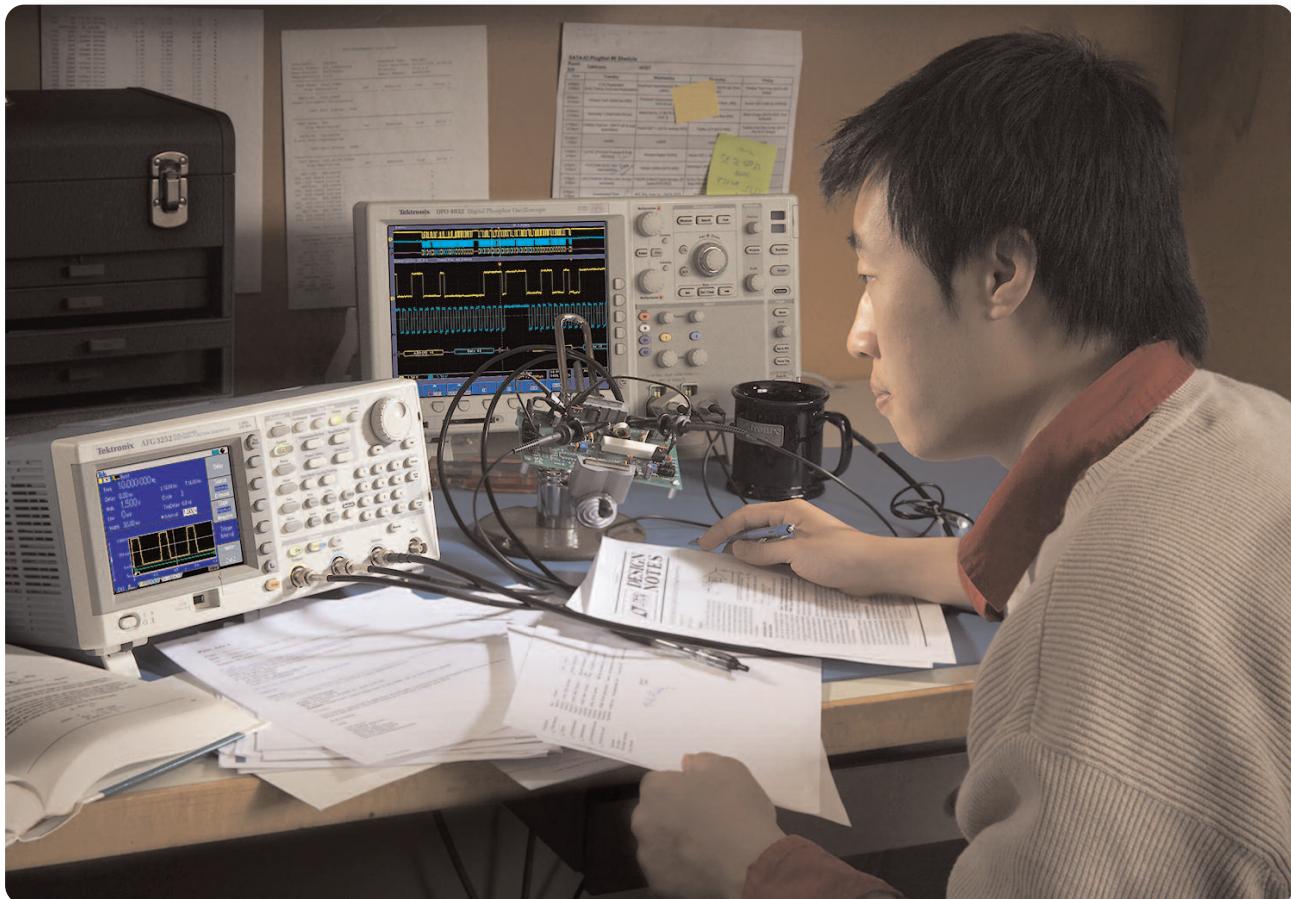


# Testing with Versatile Pulse Generation Solutions



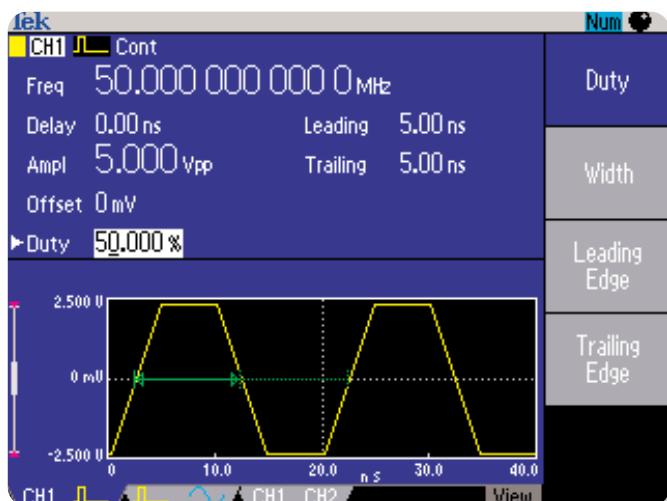
## Introduction

During the design of electronic components and circuits for computers, peripherals and serial communication, pulse pattern generators are likely the first tool considered for device characterization and functional test. Dedicated pulse pattern generators

offer various pulse formats such as double pulse, RZ and NRZ, and low jitter. For many applications, however, modern general-purpose arbitrary/function generators (AFGs) frequently present a very flexible, versatile and more affordable solution to generate pulses.

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### ► Application Note



► Figure 1. Pulse waveform screen of the AFG3252.

AFGs are perfectly suited to generate logic, trigger, and clock signals, via clock multiplier even supporting high-speed serial standards such as PCIe and SATA. This application note explores typical pulse generator test scenarios using AFGs:

- Measuring Propagation Delay and Signal Transition Time
- Characterizing Setup and Hold Time
- Evaluating Slew Rate Performance of Operational Amplifiers
- Generating Pulses with Noise or Jitter for Stress Testing
- Generating Pulses with Complex Shapes
- Simulating Low Speed Serial Signals

Specification	AFG3251/52
Number of Channels	1 / 2
Pulse Frequency	1 mHz to 120 MHz
Variable Leading Edge Time	2.5 ns to 625 s
Variable Trailing Edge Time	2.5 ns to 625 s
Pulse Width	4.00 ns to 999.99 s
Pulse Period	8.33 ns to 1000 s
Pulse Duty	0.001% to 99.999%
Lead Delay	0 ps to Period – [Pulse width + 0.8 * (Leading Edge Time + Trailing Edge Time)]
Overshoot (typical)	< 5%
Amplitude, 50 Ω Load	50 mV <sub>p-p</sub> to 5 V <sub>p-p</sub>
Amplitude, Open Circuit	100 mV <sub>p-p</sub> to 10 V <sub>p-p</sub>
Jitter (RMS, typical)	100 ps
Internal Frequency Reference	±1 ppm

► Table 1. Pulse specifications of the AFG3251/52.

These application examples are based on the AFG3251 and AFG3252 models of the AFG3000 Series. These models support single and dual channel pulse generation capability up to 120 MHz, independently adjustable rise and fall times as short as 2.5 ns, built-in noise and jitter sources, and the capability to generate pulses with complex shapes and low speed serial patterns.

### Benefits of Using Arbitrary/Function Generators for Pulse Generation

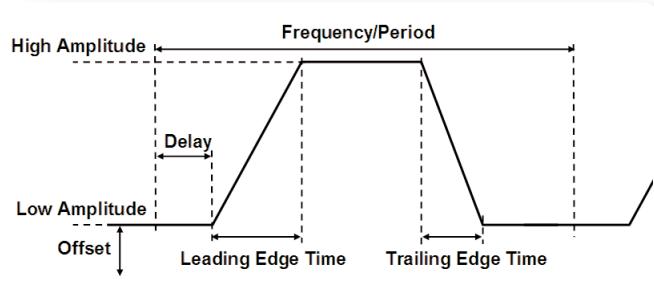
Activating the pulse generator function of the AFG3000 Series is as simple as pressing the Pulse button on the front panel. This brings all relevant waveform parameters, and a graphical depiction of the pulse waveform on screen to confirm the active settings.

Table 1 summarizes the pulse related capabilities of the AFG3251/52.

All pulse related settings (see Figure 2) are quickly accessible via dedicated shortcut keys on the front panel, and are adjustable on the fly via rotary knob or numeric key pad. During timing parameter adjustments, the output signal remains free from glitches or dropouts, which is important, for example, when characterizing devices over a sweeping clock frequency.

Dual channel models are available to support applications that require more than one input signal. Since the AFG3000 Series is based on Direct Digital Synthesis (DDS), signal shape and frequency can be selected completely independently in both channels. The signals can also be locked together in frequency and/or amplitude. In this case, an adjustable phase delay between both channels can be introduced, which is extremely useful for measuring channel to channel timing differences in semiconductor devices.

For stress testing of devices, noise can be added to pulse signals and jitter to square waves without the need for a separate function generator, as is the case for dedicated pulse pattern generators.



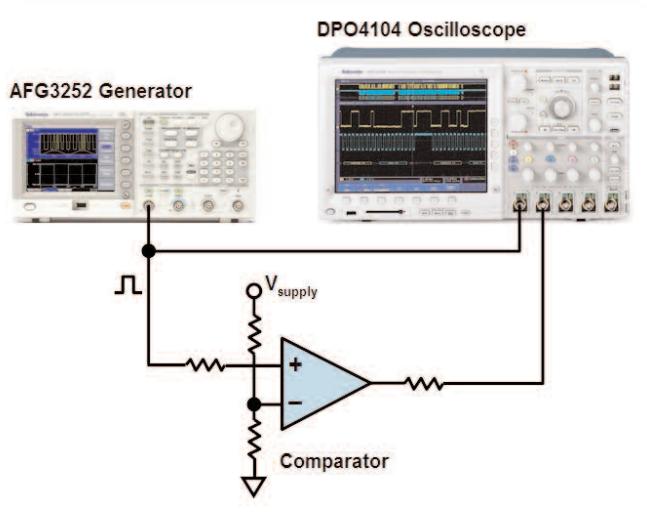
► **Figure 2.** Adjustable pulse parameters on the AFG3000 Series.

Engineers who work on a variety of designs benefit from the versatility of AFGs. Aside from pulse and square waves, the AFG3000 Series also excels at generating sine, ramp, and arbitrary waveforms, as well as seven other standard functions.

One point to consider when comparing AFGs with dedicated pulse pattern generators is that relative jitter increases with frequency due to the DDS architecture. For the AFG3251 and AFG3252, the pulse jitter specification of 100 ps implies a relative jitter of 0.01% at 1 MHz, but 1% at 100 MHz.

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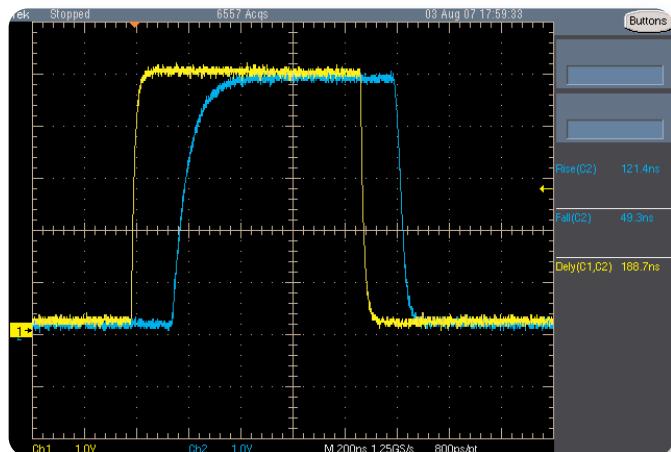


► Figure 3. Measurement setup for propagation delay measurement.

### Measuring Propagation Delay and Signal Transition Time

In logic devices such as buffers and comparators, a parameter of interest is the propagation delay or response time, i.e. the time it takes for the device output to respond to an input signal. To measure this parameter, use an AFG3251 or AFG3252 to stimulate the device input with a pulse signal, and measure device input and the output signal with an oscilloscope.

Program the signal source to generate pulses of a frequency and amplitude within the operating range of the device. As an example, the following provides instrument settings and measurement results for the comparator model LM393.

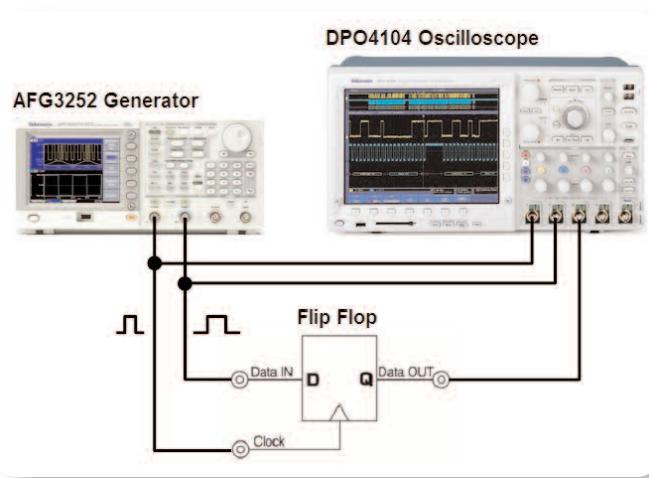


► Figure 4. Oscilloscope screen of propagation delay measurement.

Parameters	Setting
Run Mode	Continuous
Function	Pulse
Frequency	500 kHz
Leading/Trailing Edge	2.5 ns
Amplitude High	5 V
Amplitude Low	0 V

► Table 2. AFG3251/52 settings for comparator characterization.

The yellow trace in Figure 4 depicts the input signal to the device and the blue trace the output signal. The oscilloscope measured a response time of 188.7 ns, a signal output rise time of 121.4 ns and a fall time of 49.3 ns.

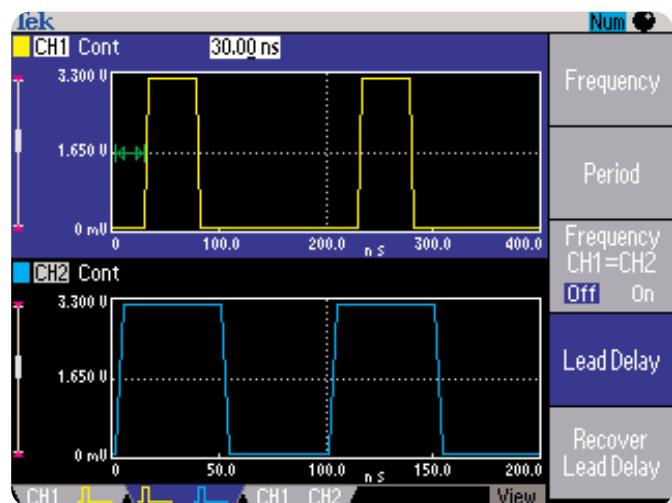


► Figure 5. Measurement setup for flip-flop characterization.

### Characterizing Setup and Hold Time

In logic circuit timing, setup time and hold time conditions play a critical role. A logic circuit captures data at the leading edge of the clock. For the data to be captured correctly, it needs to settle a certain time before the clock edge and remain stable for a certain time after this edge. The necessary settling time before the clock edge is known as setup time and the necessary time after the clock edge is known as hold time.

These values are specified in the datasheet of the logic IC. They vary with the voltage of the power supply and other conditions. Necessary tools to measure setup and hold times are a dual-channel AFG and an oscilloscope.



► Figure 6. AFG3000 screen – Waveform View.

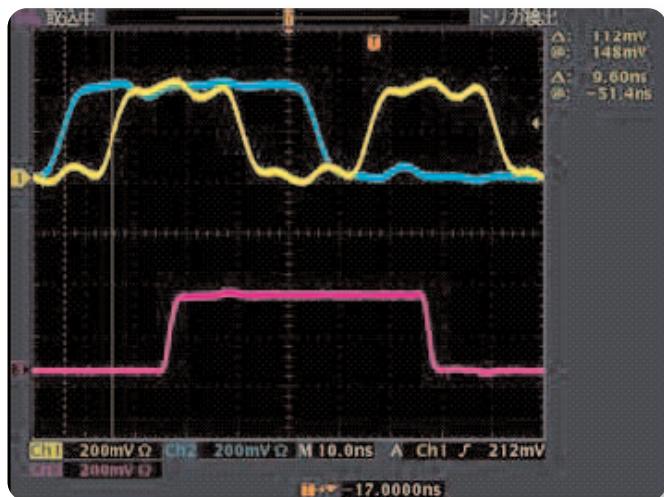
Parameters	Setting
Run Mode	Continuous
Channel 1 - Function	Pulse
Channel 1 - Frequency	5 MHz
Channel 2 - Frequency	10 MHz
Channel 1/2 - Amplitude High	3.3 V
Channel 1/2 - Amplitude Low	0 V

► Table 3. AFG3252 Settings for flip flop characterization.

To stimulate the device, program the AFG3252 with the settings in Table 3. Channel 1 generates the clock and channel 2 the data. To synchronize data and clock timing, press the Phase/Delay button and then Align Phase in the soft menu on the screen. The clock,

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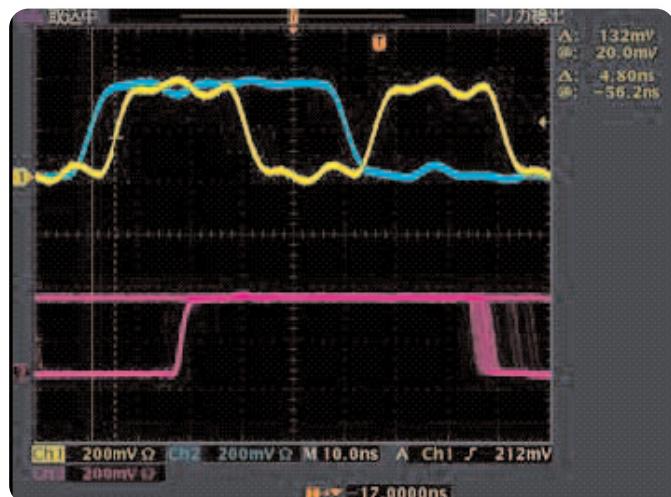
### ► Application Note



► Figure 7. Sufficient setup time.

data and device output signals are measured with an oscilloscope.

To determine setup and hold time, press the Delay button on the AFG3252 front panel and vary the delay of channel 1 with the rotary knob while observing the flip flop output signal on the oscilloscope. The delay can be adjusted in increments as small as 10 ps via the rotary knob.



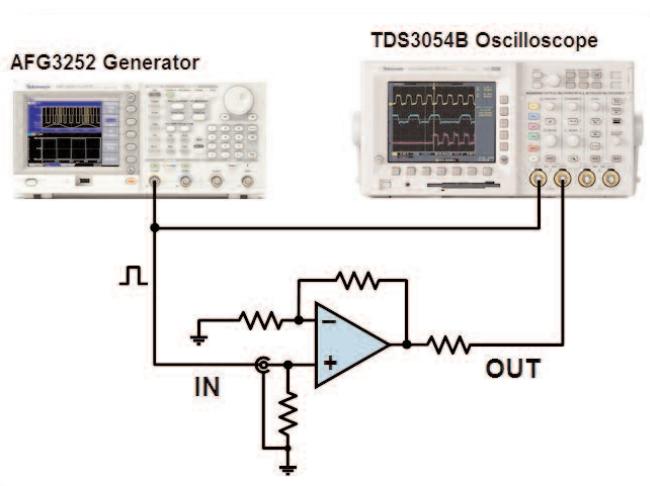
► Figure 8. Insufficient setup time.

Figure 7 shows input and output signals of the flip flop for a sufficient setup time. The yellow trace represents the clock input, the blue trace the data input and the magenta trace the data output. For the selected setup time of 10 ns the data input is captured at the clock's rising edge and output properly.

Figure 8 shows the flip flop signals for a setup time of 5 ns which is insufficient. The data output fluctuates here between high and low level, because the data input is changing its level, while the flip-flop circuit is still processing the data. The output develops a metastable state (neither high level nor low level).

### Evaluating Slew Rate Performance of Operational Amplifiers

High-speed operational amplifiers (op amps) are among the most common analog components in use today. They can be found in television sets, set-top boxes, video broadcast equipment, wireless communications base stations, fiber-optic products, radar systems, satellite receivers, card readers, bar code scanners, and many other areas.



► Figure 9. Measurement setup for op amp slew rate characterization.

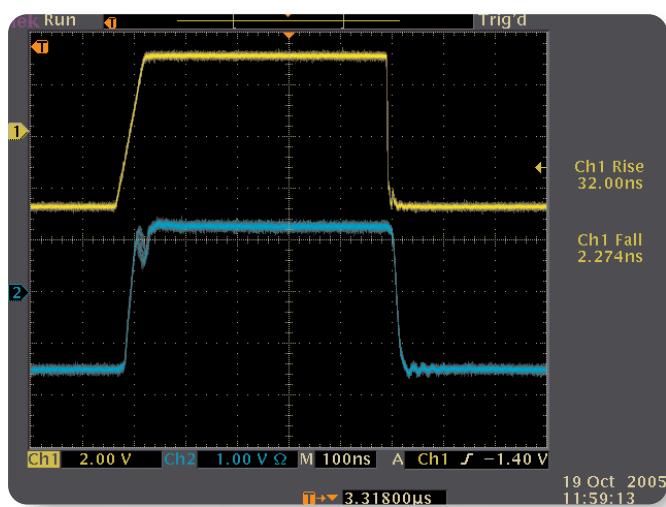
Parameters	Setting
Run Mode	Continuous
Function	Pulse
Frequency	1 MHz
Amplitude	5 V <sub>p-p</sub>

► Table 4. AFG3251/52 settings for op amp characterization.

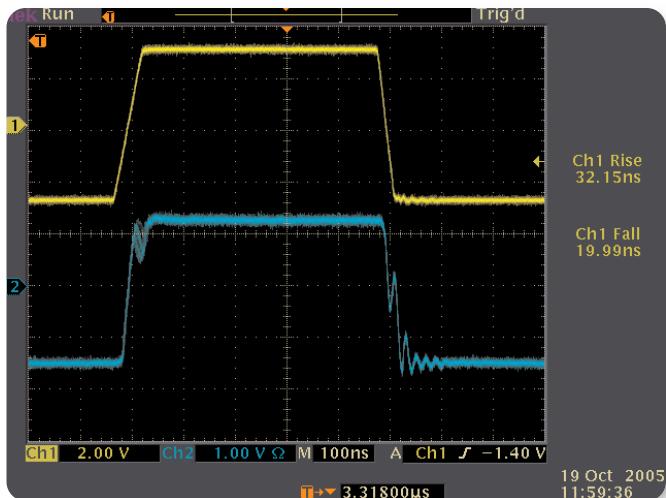
A critical performance aspect of op amps is their transient response or slew rate performance. Op amps used in set-top boxes and security video applications need a high slew rate combined with ultra-low distortion. Slew rate and transient response are also an issue for op amps that drive extremely fine movement in ink jet printers and medical devices.

The op amp's transient response may be different for the rising and falling edges of the input signal, a behavior known as asymmetrical slew rate performance. It may affect whether the op amp is used in an inverting or non-inverting configuration. Knowing the timing characteristics of an op-amp makes it possible to optimize gain and feedback resistors, or take other measures to achieve the desired circuit behavior.

To characterize an op amp's slew rate performance,



► Figure 10. At an input signal rise time of 32 ns the op amp output signal starts to oscillate.

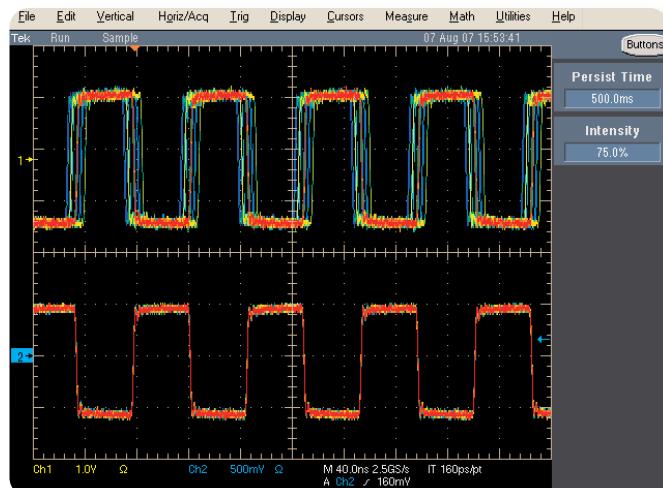


► Figure 11. Increasing the fall time. The trailing edge of the output begins to oscillate at some point.

measure its transient response with an oscilloscope while stimulating its input with a pulse signal with variable rise time, fall time, and amplitude. The pulse generation solution used must provide independent control over these parameters. The Tektronix AFG3000 Series delivers this flexibility, along with ample bandwidth and precision to ensure accurate results.

## Testing with Versatile Pulse Generation Solutions

### ► Application Note

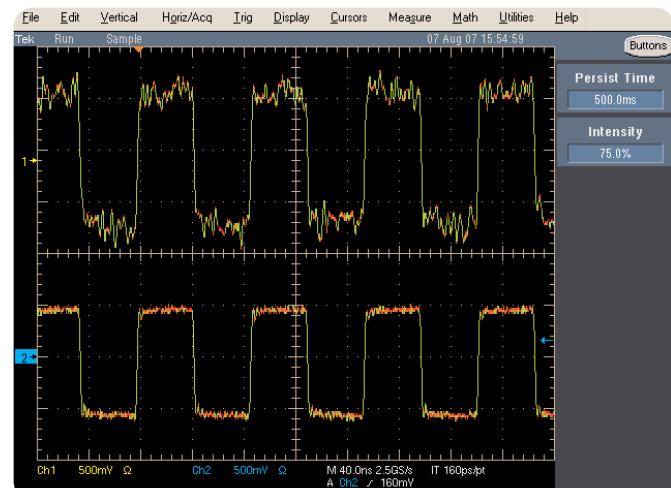


► **Figure 12.** Pulse with controlled jitter (upper trace) and without jitter (lower trace).

Figure 9 shows the measurement setup. The example discussed here is using a 220 MHz high-speed op amp intended for video line driver applications.

After entering the basic waveform settings into the signal source according to Table 4, hold the trailing (falling) edge constant at 2.5 ns, and increase the leading (rising) edge gradually from the minimum setting of 2.5 ns while observing the op amp output signal on the oscilloscope. In the example here, the output signal starts to oscillate when the rise time reaches 32 ns (Figure 10).

Next, keep the leading edge time constant at 32 ns and slowly increase the trailing edge time starting from 2.5 ns. As Figure 11 reveals, the op amp output starts to oscillate at a falling edge time of approximately 20 ns. Clearly this op amp has asymmetrical characteristics.



► **Figure 13.** Pulse with added noise (upper trace) and without added noise (lower trace).

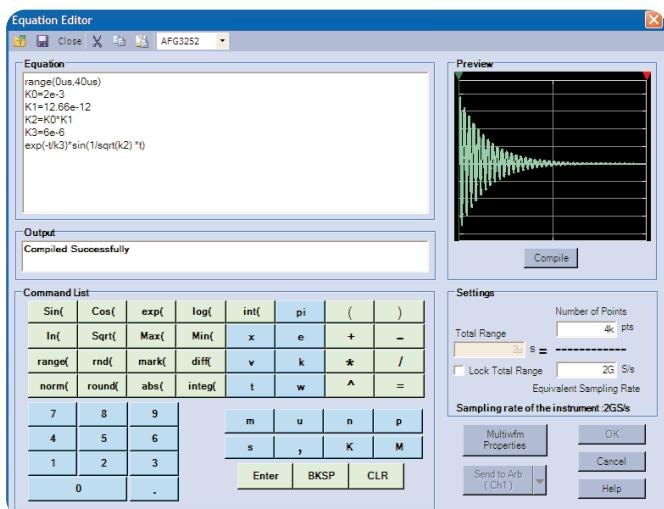
Parameters	Setting
Run Mode	Modulation
Function	Square
Modulation Type	PM
PM Frequency	2 mHz to 50.00 kHz
Modulation Shape	Selectable
Deviation	0.0° to 180.0°

► **Table 5.** AFG3251/52 settings for jitter generation.

### Generating Pulses with Jitter or Noise for Stress Testing

To assure reliable operation, digital components and circuits need to be robust against a certain amount of jitter and noise in clock and data signals. Otherwise, communication errors or system failures could result. To evaluate components and circuits for their jitter and noise tolerance, electronic design engineers need a solution that can generate pulses with controllable jitter and noise.

While dedicated pulse pattern generators typically



► **Figure 14.** Equation Editor in waveform editing software ArbExpress for creating complex pulses and other waveforms.

require a separate function generator to add signal distortion, the AFG3000 Series provides a one box solution with jitter and noise generator built into the instrument.

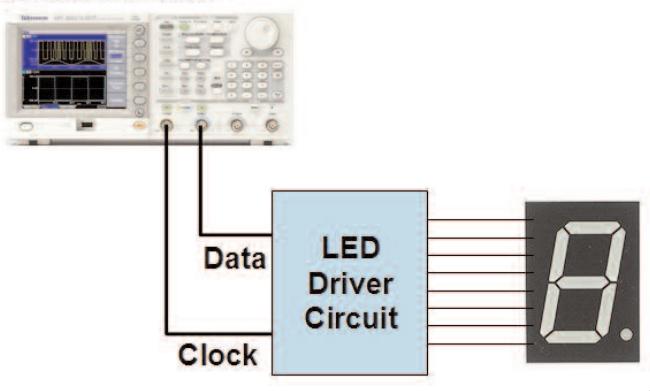
Jitter can be added via the built in phase modulator with selectable modulation frequency, wave shape, and phase deviation. After you program the instrument with the settings in Table 5, the instrument will output a pulse

with 50% duty cycle and well-defined jitter.

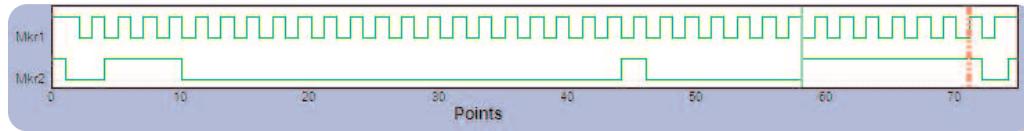
## Testing with Versatile Pulse Generation Solutions

### ► Application Note

#### AFG3252 Generator



► **Figure 15.** Measurement setup for I2C controlled LED-driver.



► **Figure 16.** ArbExpress marker pane with I2C clock and data signal.

To add noise to any generated signal, simply select the Output Menu after you press the desired waveform button and turn on Noise Add. The noise level can then be selected from 0% to 50%. Please note that Noise Add reduces the signal amplitude by half to prevent the noise from clipping at amplitude settings close to the maximum.

### Generating Pulses with Complex Shapes

Some applications, as diverse as radar test, magnetic storage device test and laser spot welding, require electrical pulses with complex shapes. Aside from rectangular pulses, the AFG3000 Series provides the following standard pulse shapes:  $\text{Sin}(x)/x$ , Gaussian, Lorentzian, Exponential Rise and Fall. In cases, where other pulse shapes are needed, you can use the arbitrary waveform function of the AFG3000 Series and program the desired pulse shape via mathematical equations or freehand drawing in the waveform editing

software, ArbExpress.

Creating pulse waves via arbitrary waveform functions works well with DDS-based arbitrary/function generators as long as the selected pulse repetition rates are well below the instrument's clock rate. With a clock rate of 2 GS/s and 500 ps jitter (rms), the AFG3252 supports a wide range of applications. However, at higher pulse repetition rates, the waveform point skipping and duplication inherent to DDS-based generators can lead to extra jitter.

### **Simulating Low Speed I2C Serial Signals**

Micro-controllers and computers in embedded systems often utilize low-speed serial buses such as I2C, SPI, RS-232, CAN and LIN to communicate with specialized devices such as sensors, switches, a/d-converters, digital potentiometers and displays. To validate and stress test new designs, engineers may need to simulate data and clock signals. The following application illustrates how I2C bus signals that control a driver for a numerical LED can be easily created and generated with a dual-channel arbitrary/function generator.

As the block diagram in Figure 15 shows, channel 1 of the AFG3252 generates the clock and channel 2 the

Parameters	Setting
Run Mode	Continuous
Function Channel 1/2	Arb
Frequency CH1=CH2	On
Frequency	1 kHz
Amplitude – Level CH1=CH2	On
Amplitude – High Level	2 V
Amplitude – Low Level	0 V
Channel 1 – Arb – Arb Waveform Menu	User 1
Channel 2 – Arb – Arb Waveform Menu	User 2
Output Channel 1/2	On

► **Table 6.** AFG3252 settings for I2C signal generation.

data signal.

Data and clock signals are created via the marker functions of the software package ArbExpress. After launching the application, select Standard Waveform in the File menu, select DC as function in the Standard Waveform window that opens and set the wavelength to the desired number of points. In the new Wavebook window that opens, enter the clock and data waveforms in the marker pane via the right-click mouse functions.

After clock and data signal are created, save the waveform file in .csv format. Then open this .csv file

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